What Is Claimed Is:

1. A semiconductor system having a p-n junction, which takes the form of a substrate having an edge region, which is made up of a first layer (3) of a first conductivity type and a second layer (1, 2, 4) of the opposite conductivity type, the second layer (1, 2, 4) being made up of at least two sublayers (1, 2), the first sublayer (2) having a first dopant concentration and the second sublayer (1) having a second dopant concentration that is lower than the first dopant concentration, both sublayers (1, 2) together with the first layer (3) forming a p-n junction, the p-n junction of the first layer (3) with the first sublayer (2) being formed exclusively in the interior of the chip and the p-n junction between the first layer (3) and the second sublayer (1) being formed in the edge region of the chip, and the second layer (1, 2, 4) including a third sublayer (4) having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration,
wherein the third sublayer (4) over the largest part of its cross-sectional area (BC) in the interior of the semiconductor system (20, 30) borders immediately on the first sublayer (2), while bordering on the second sublayer (1) only in a comparatively narrow edge region of the cross-sectional area (BC).

2. The semiconductor system as recited in Claim 1, wherein the sublayers (2, 4) of the semiconductor system (20, 30, 60) at least touch in a central region of the semiconductor system (20, 30, 60), but preferably overlap in regions.

3. The semiconductor system as recited in one of Claims 1, 2,
wherein the dopant concentration in each of the sublayers (2, 4) is higher than the dopant concentration in the sublayer (1) forming the basic substrate.

4. The semiconductor system as recited in one of Claims 1 through 3,
wherein in its central region the sublayers (2, 3) form a first p-n junction (2-3) between p+-doped and n+-doped semiconductor substrate.

5. The semiconductor system as recited in one of the preceding claims,
wherein in its edge region the sublayers (1, 3) form a second p-n junction (1-3) between p+-doped and n--doped semiconductor substrate.

6. The semiconductor system as recited in one of the preceding claims,
wherein it has in its edge region a wide, shallow sawing trench having a sawing width (SB) and a sawing depth (ST), the sawing width (SB) being greater than 80 micrometers, preferably greater than 100 micrometers, and the ratio of sawing width (SB) to sawing depth (ST) having a value > 3.

7. The semiconductor system as recited in one of the preceding claims,
wherein the sawing trench (SB, ST) is completely filled with solder material in such a way that the wall surfaces of the sawing trench are covered by solder material and are protected by this solder material.

8. The use of the semiconductor system as recited in one of the preceding claims as an electric valve (diode).

9. The semiconductor system as recited in one of the preceding claims,
wherein the breakdown voltage (UZR) in the edge region of the semiconductor system (20, 30, 60) is significantly greater than the breakdown voltage (UZM) in a central region of the semiconductor system (20, 30, 60).

10. The semiconductor system as recited in Claim 9,
wherein the breakdown voltage in the edge region (UZR) is greater than the breakdown voltage (UZM) approximately by a factor of 2 to 7.

11. The semiconductor system as recited in one of Claims 1 through 10,
wherein the bulk resistance in a central region of the semiconductor system (20, 30, 60) is lower than the bulk resistance in an edge region of the semiconductor (20, 30, 60).

12. A semiconductor system having a p-n junction, which takes the form of a substrate having an edge region, which is made up of a first layer (3, 2) of a first conductivity type and a second layer (1, 4) of the opposite conductivity type, the second layer (1, 4) being made up of at least two sublayers (1, 4) the first sublayer (4) having a first dopant concentration and the second sublayer (1) having a second dopant concentration that is lower than the first dopant concentration, both sublayers (1, 4) together with the first layer (3, 2) forming a p-n junction, the p-n junction of the first layer (2) with the sublayer (4) being formed exclusively in the interior of the chip and the p-n junction between the first layer (3) and the second sublayer (1) being formed in the edge region of the chip,
wherein the layer (4) over the largest part of a cross-

sectional area (BC) in the interior of the semiconductor system (60) borders immediately on the first layer (2), while bordering on the second layer (1) only in a comparatively narrow edge region of the cross-sectional area (BC).

13. A semiconductor system having a p-n junction, which takes the form of a substrate having an edge region, which is made up of a first layer (3) of a first conductivity type and a second layer (1, 2, 4) of the opposite conductivity type, the second layer (1, 2, 4) being made up of at least two sublayers (1, 2), the first sublayer (2) having a first dopant concentration and the second sublayer (1) having a second dopant concentration that is lower than the first dopant concentration, both sublayers (1, 2) together with the first layer (3) forming a p-n junction, the p-n junction of the first layer (3) with the first sublayer (2) being formed exclusively in the interior of the chip and the p-n junction between the first layer (3) and the second sublayer (1) being formed in the edge region of the chip, and the second layer (1, 2, 4) including a third sublayer (4) having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration,
wherein the third sublayer (4) over the largest part of its cross-sectional area (BC) in the interior of the semiconductor system (20, 30) borders immediately on the first sublayer (2), while bordering on the second sublayer (1) only in a comparatively narrow edge region of the cross-sectional area (BC).

14. A method for manufacturing a semiconductor system as recited in one of Claims 1 through 13, characterized by the following method steps:

- manufacture of a semiconductor substrate of a first conductivity type forming a first sublayer (1) of a semiconductor system (20, 30),

- doping of the first sublayer (1) on both sides for forming two further sublayers (2, 4) of the same conductivity type as the first sublayer (1) but with different degrees of doping in such a way that the two sublayers touch or overlap at most in a central region of the semiconductor system (20, 30),

- production of a fourth sublayer (3) of an opposite conductivity type by introducing a dopant into the sublayers (1, 2) as well as by increasing the dopant concentration of sublayer (4),

- covering the outer surfaces of the sublayers (3, 4) with metallic contact layers (5, 6).

15. The semiconductor system as recited in one of Claims 1 through 13, characterized by the interchanging of the p-doped and n-doped layers.